

Figure 1
Prior Art

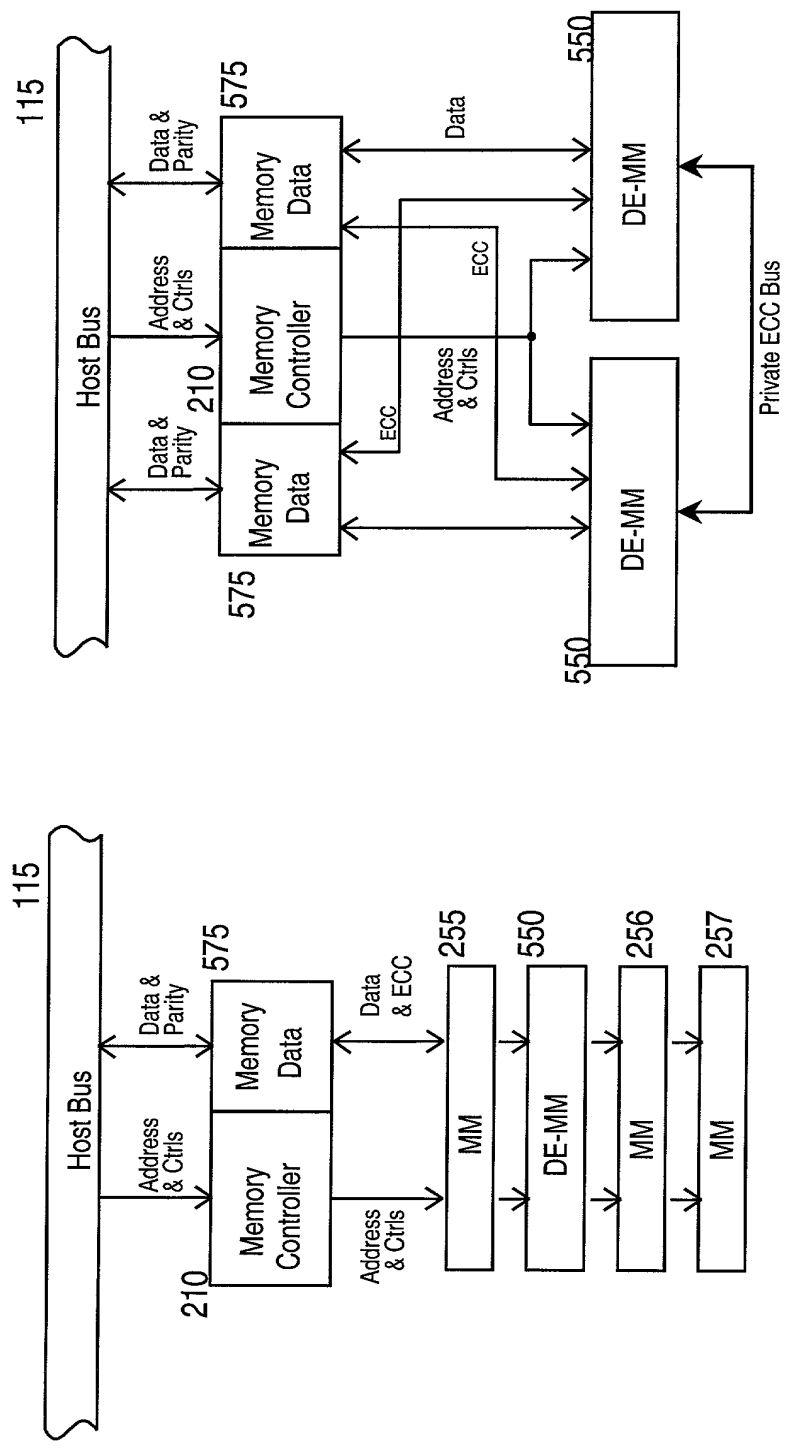


Figure 2a

Figure 2b

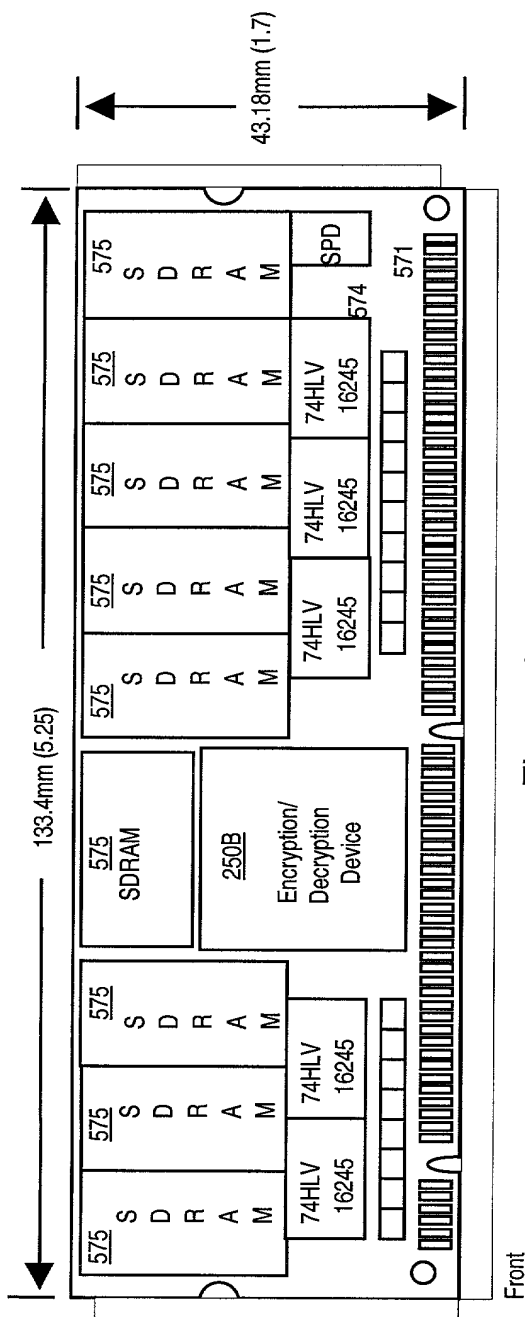


Figure 4a

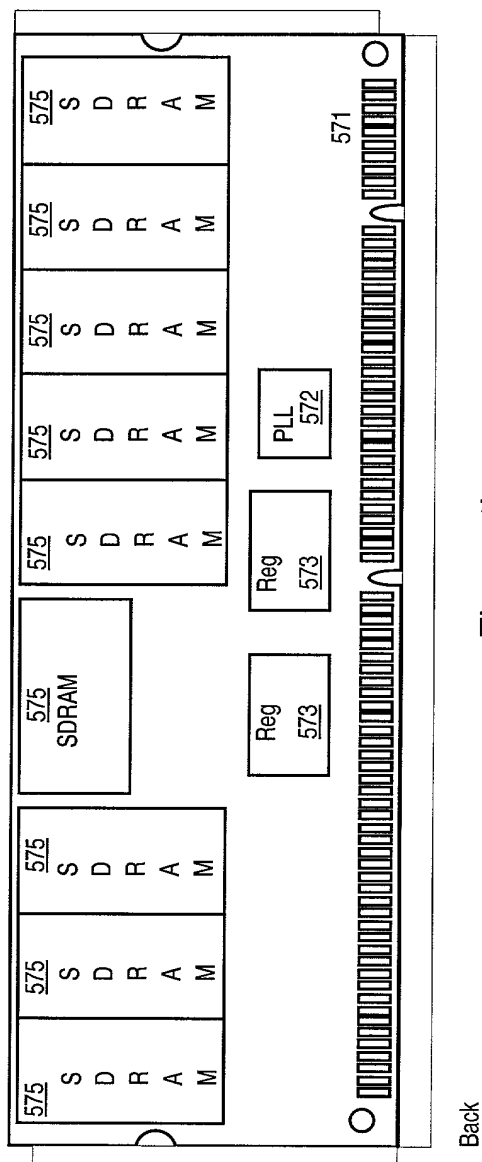


Figure 4b

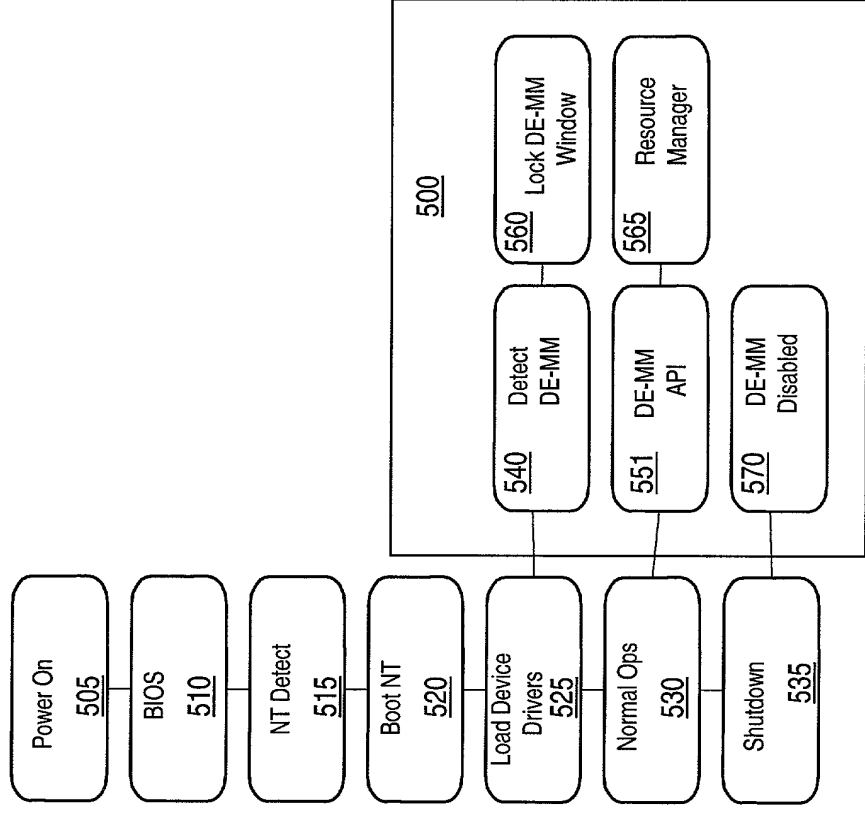


Figure 5

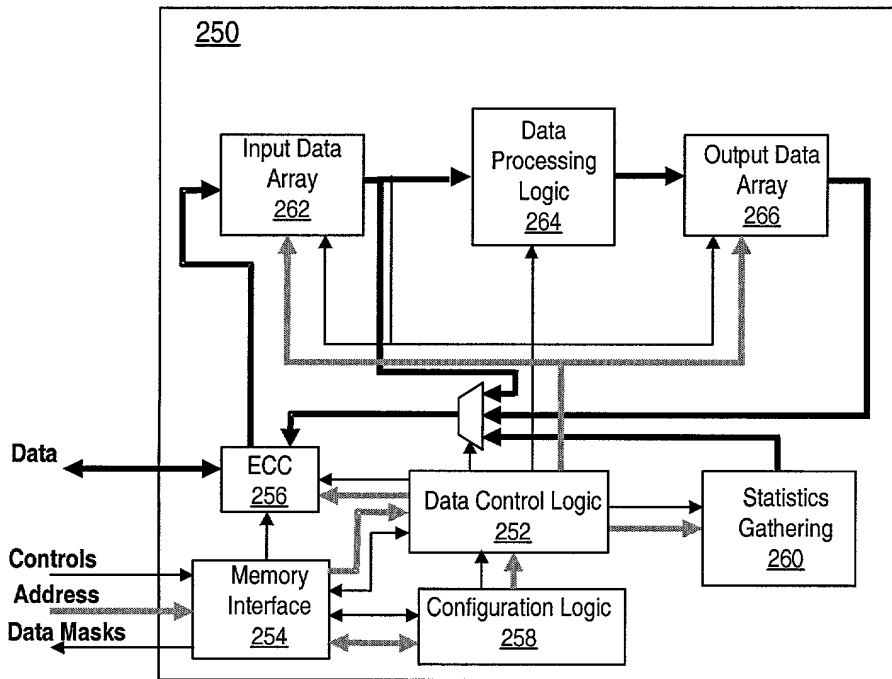


Figure 6

DE-MM device logic

09840724-042301
10E240-42204860

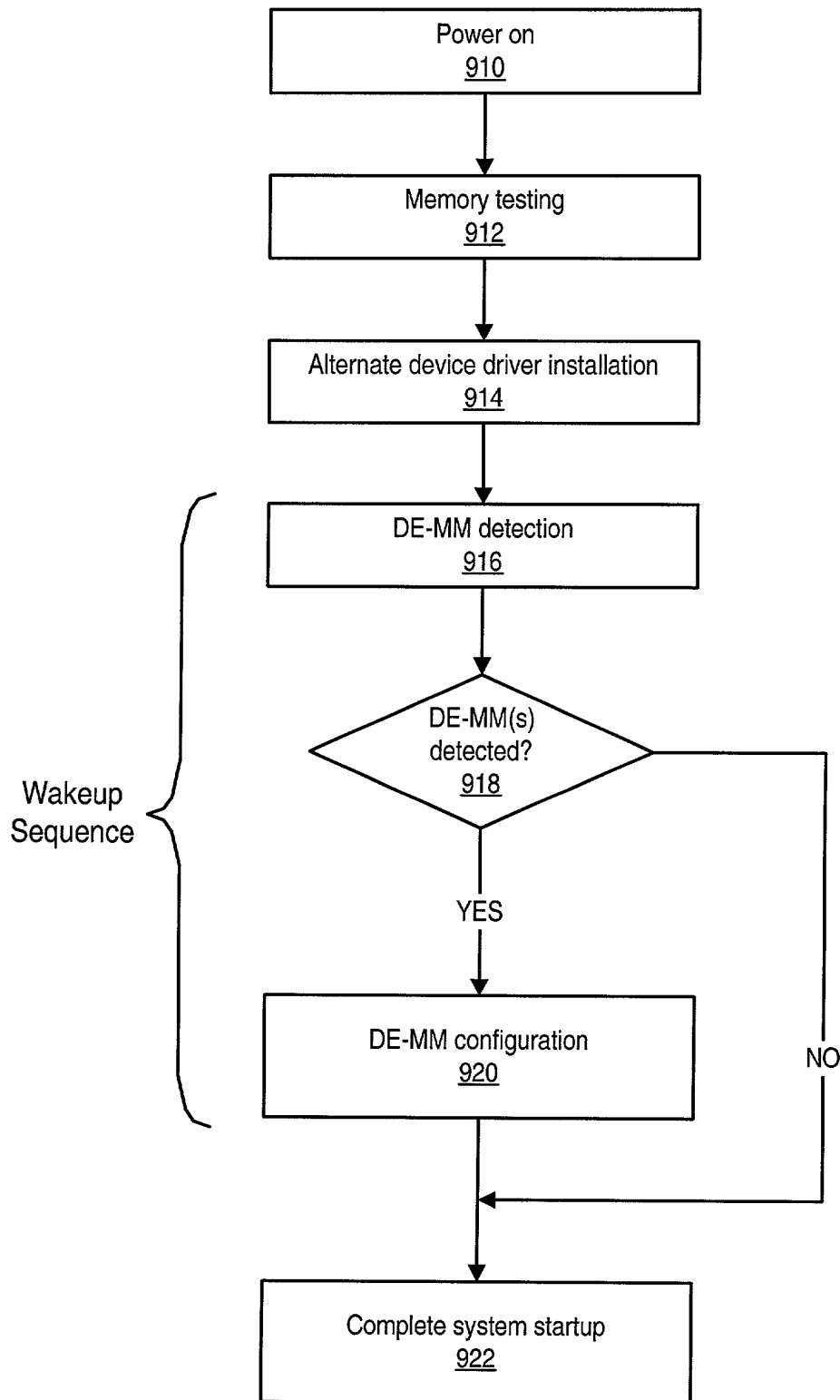


Figure 7a

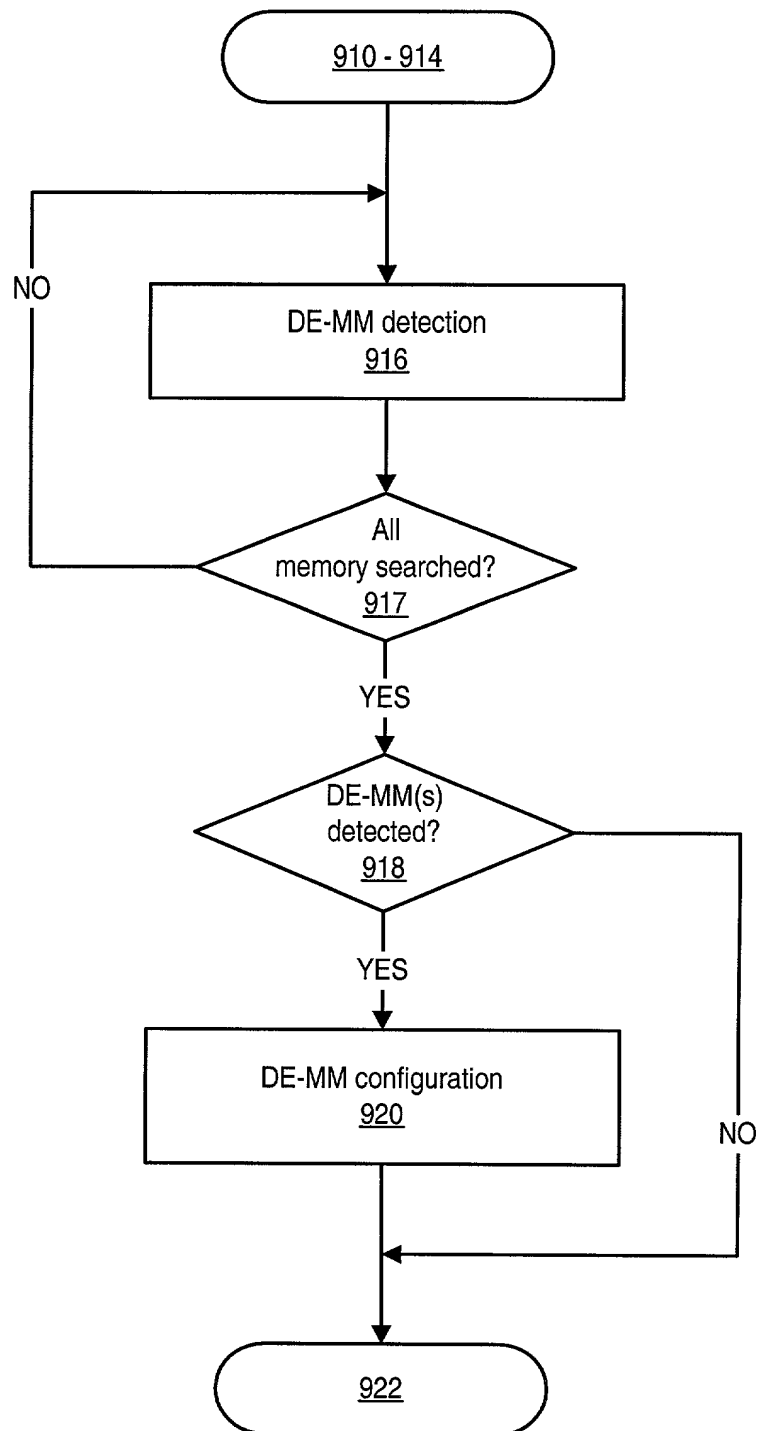


Figure 7b

09840724.042301
T0E240.42/04860

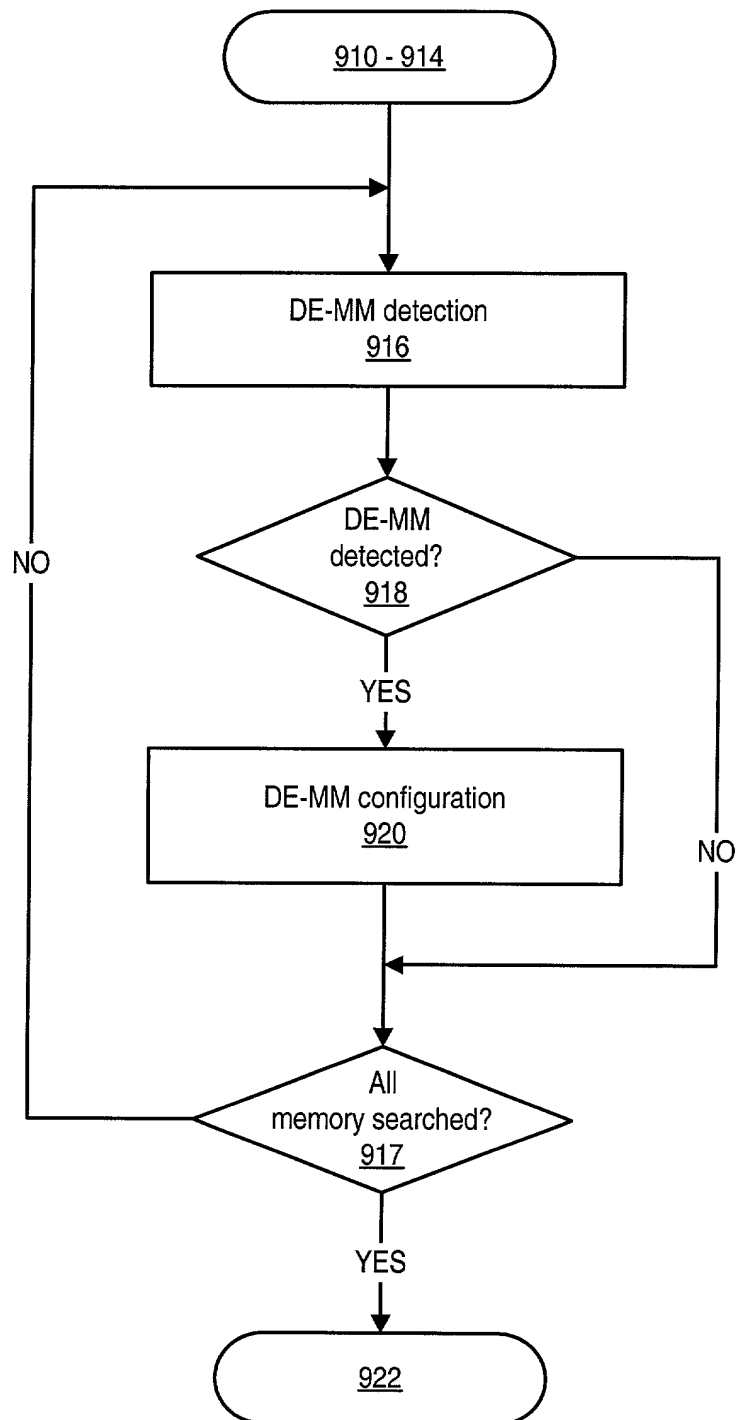


Figure 7c

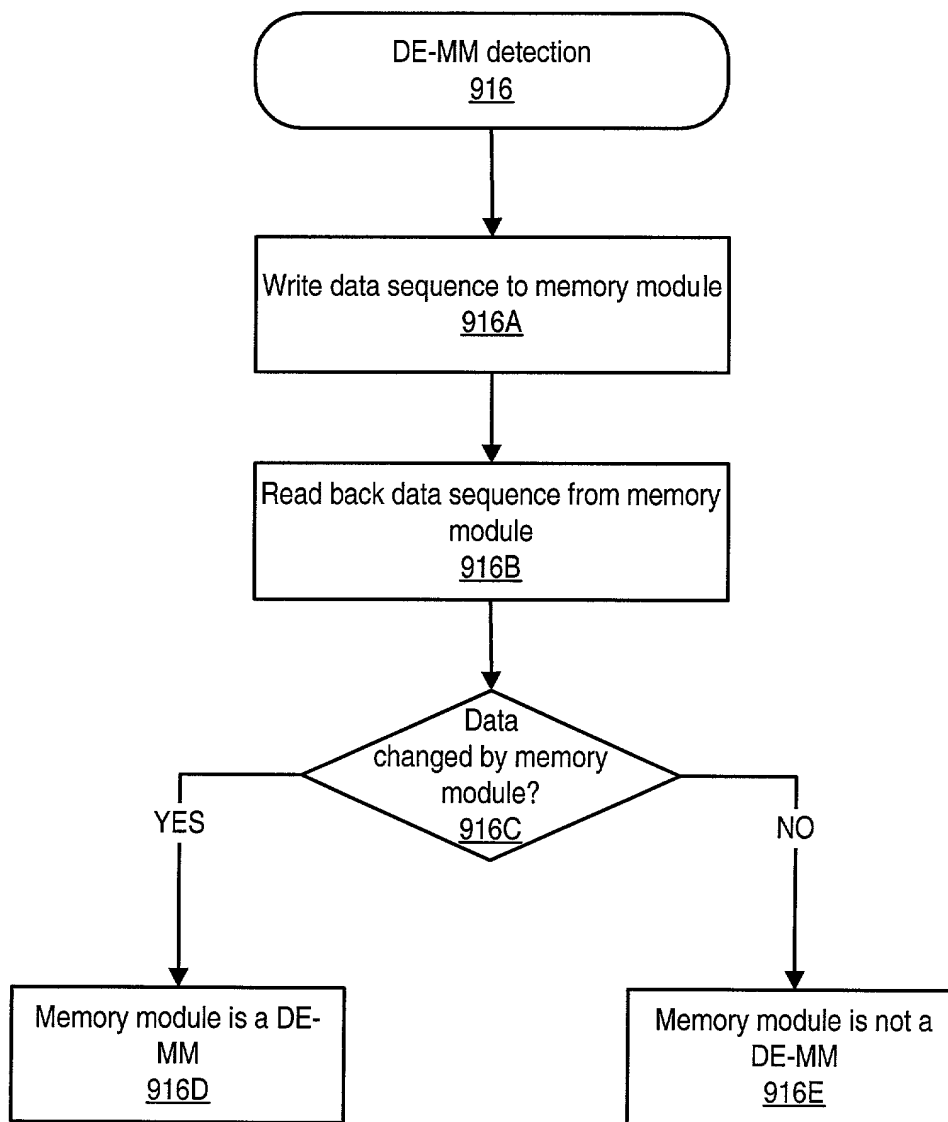


Figure 8

09340724-042301
T0E240-42-04B60

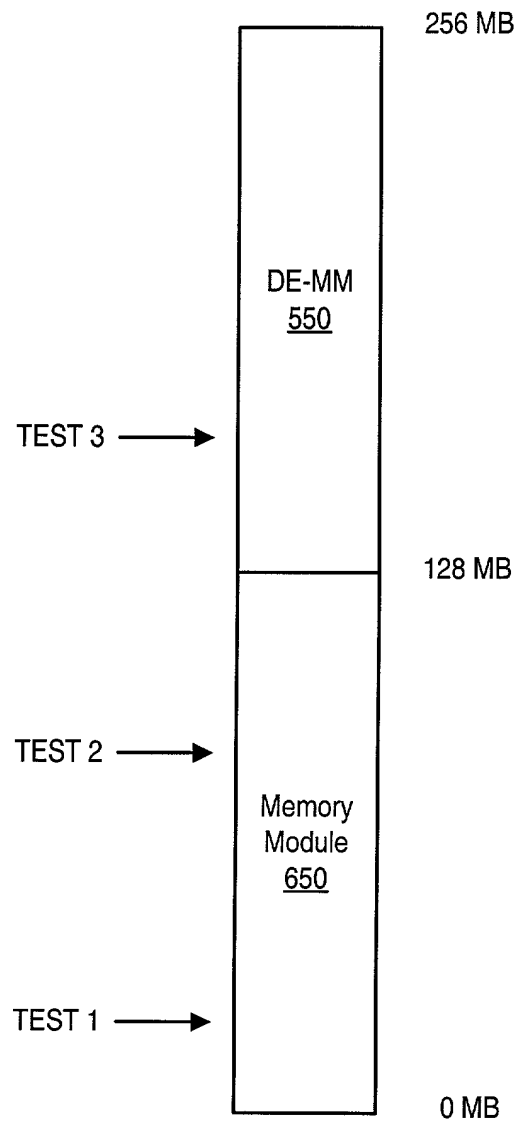


Figure 9

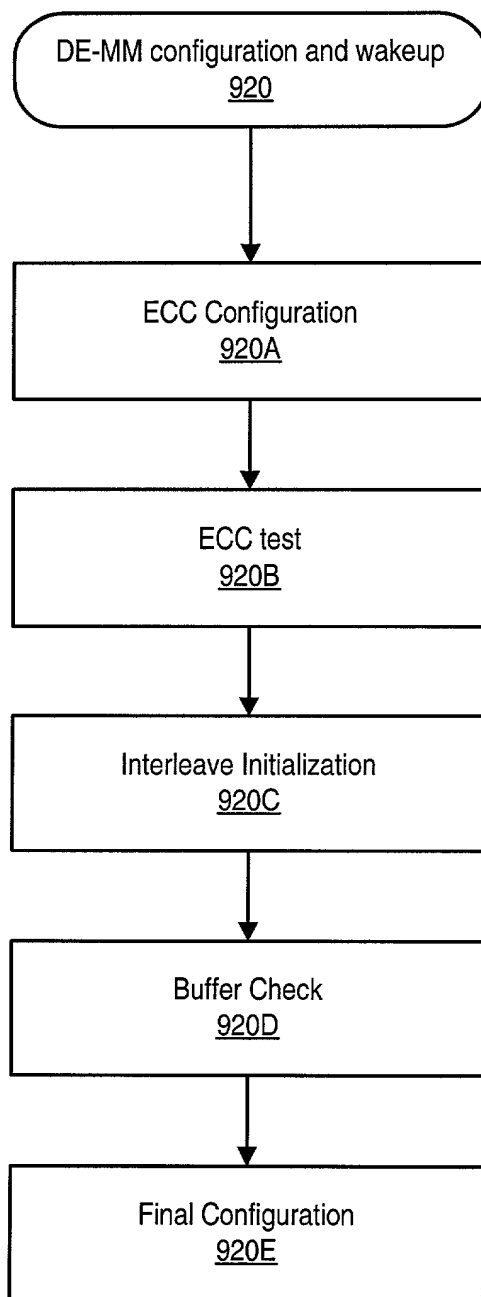


Figure 10

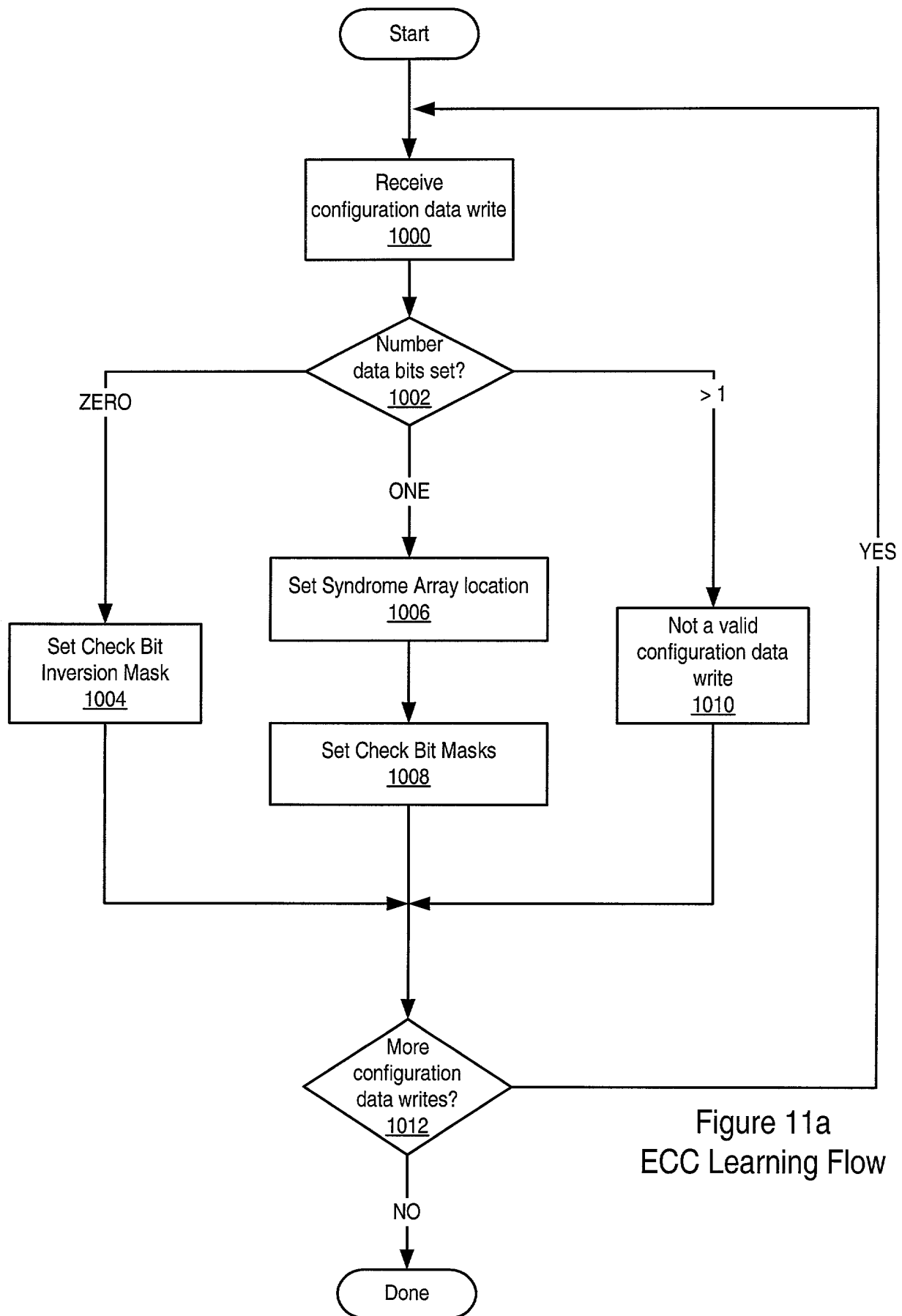


Figure 11a
ECC Learning Flow

09840724-042304
T0E240-42204860

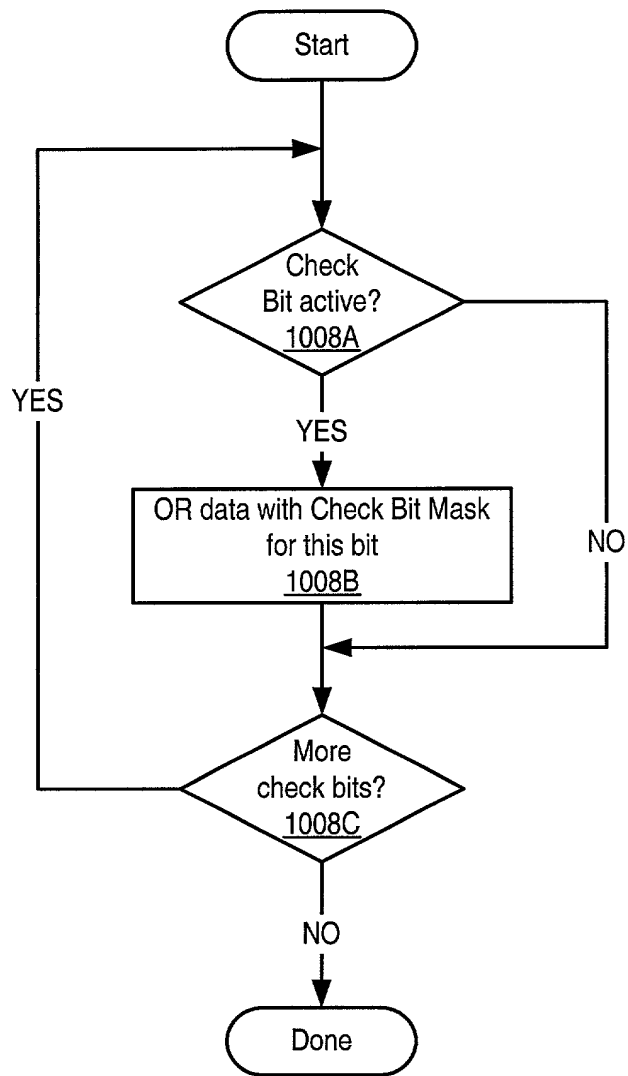


Figure 11b
Learning Check Bit Masks

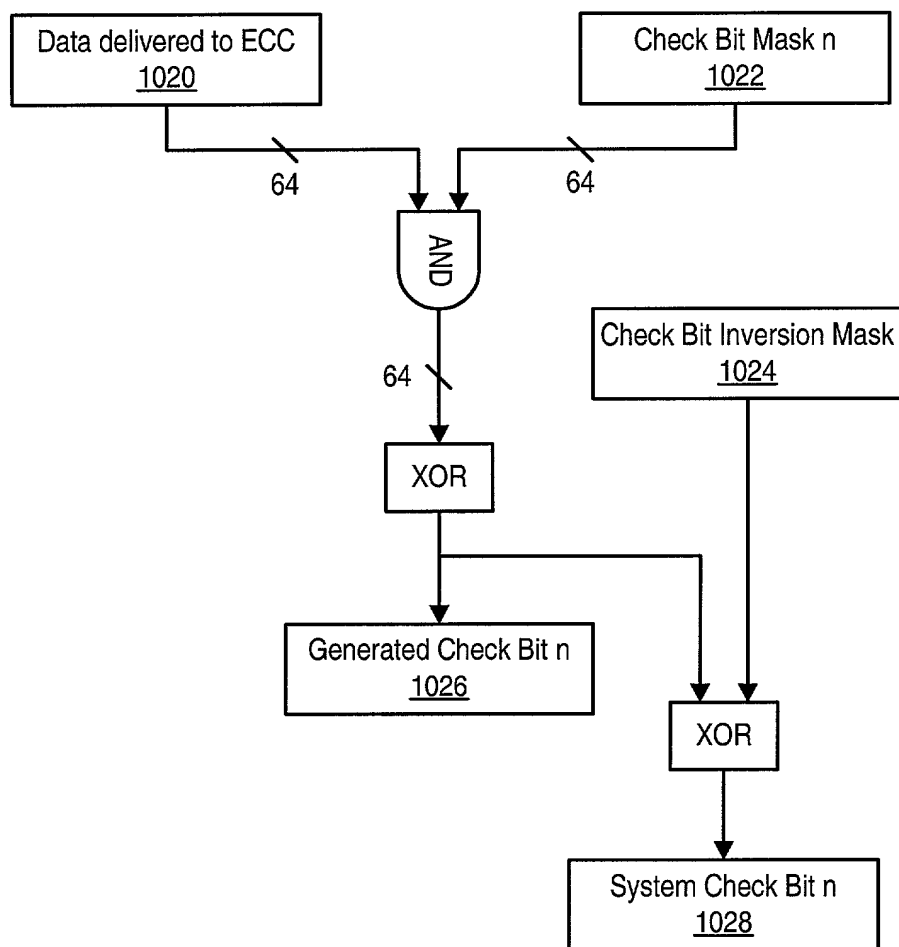


Figure 12
Check Bit Generation

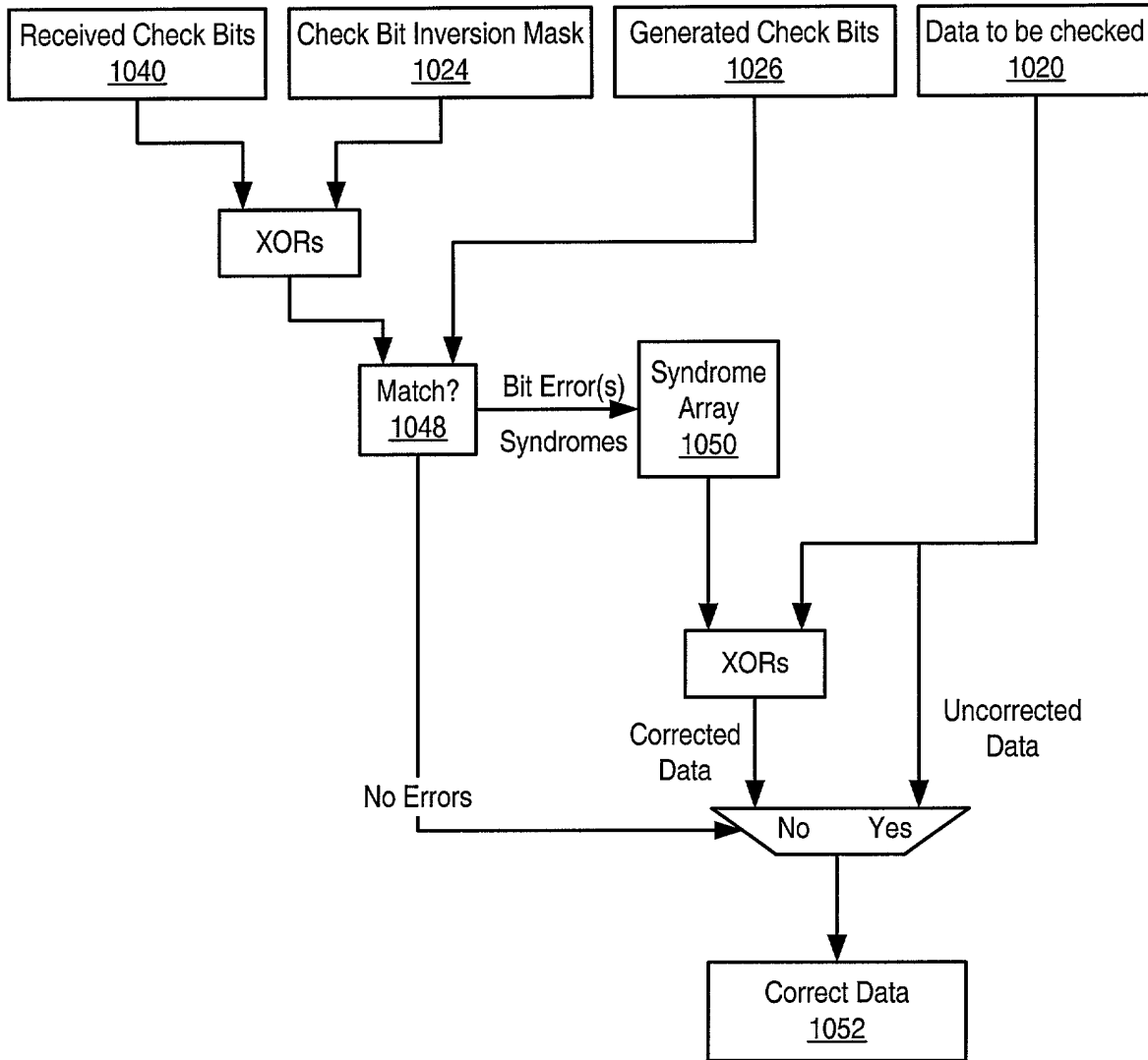


Figure 13
Data Checking and Correction

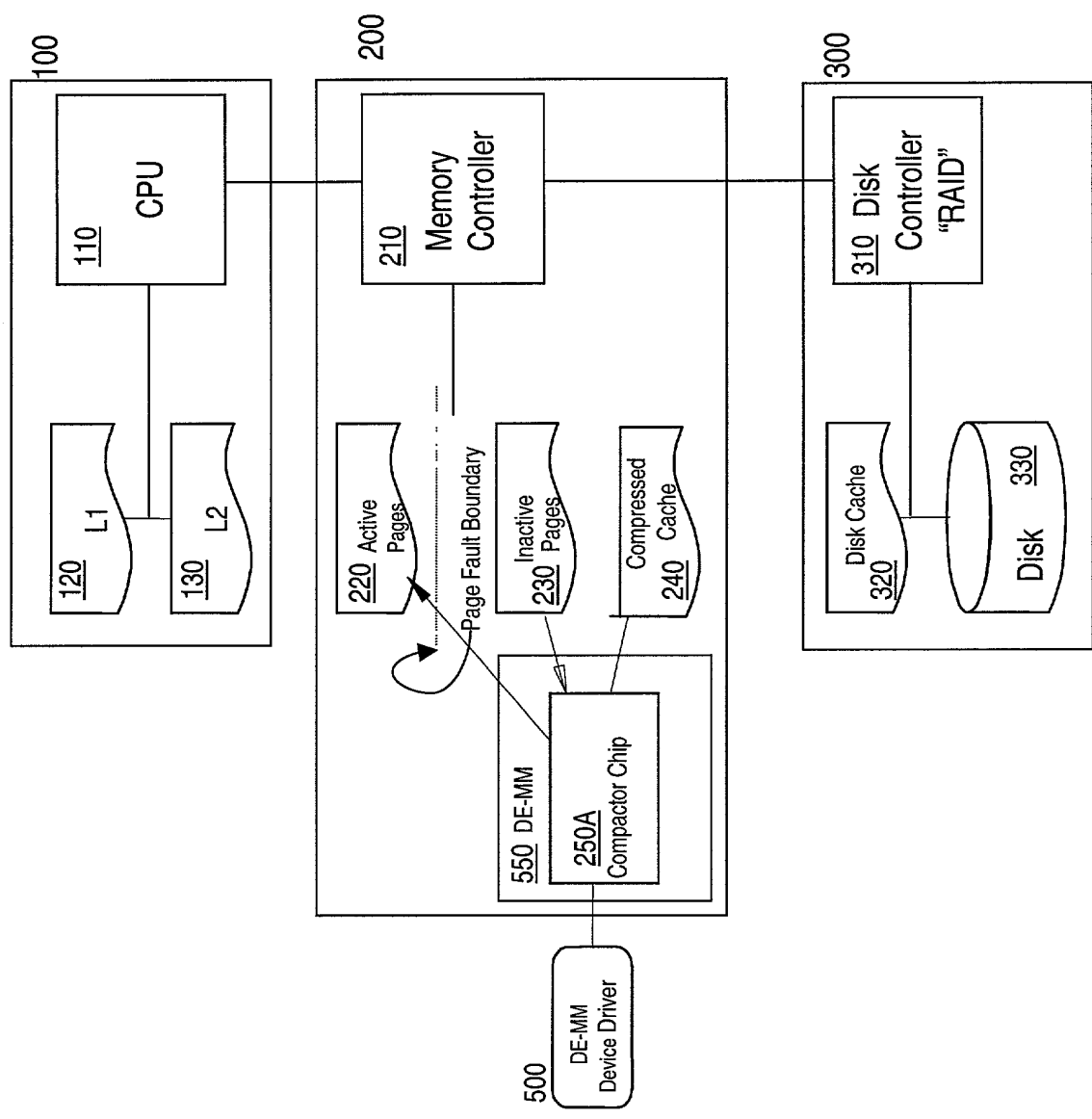


Figure 14

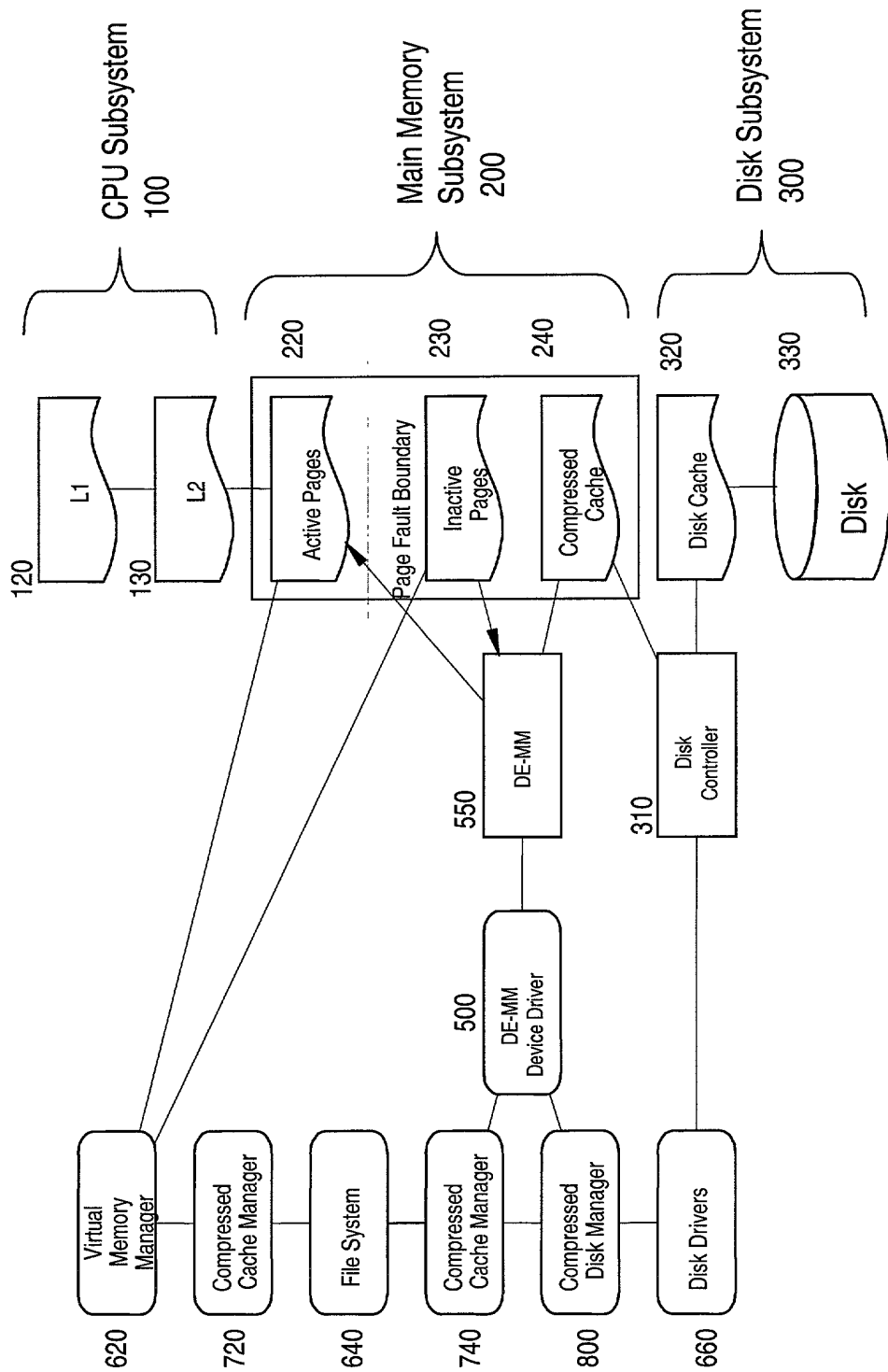


Figure 15